Fabrication of sub-μm bipolar transistor structures by scanning probe microscopy

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(Received 18 May 1998; accepted for publication 28 July 1998)

We show how sub-μm sized transistor structures (down to 50 nm cross section) can be fabricated by thermally assisted electromigration of mobile dopants inside the semiconductor $CuInSe_2$. Small device structures are fabricated by application of an electric field to the sample via the contact, defined by a conducting atomic force microscope tip. The structures are characterized by nm scale scanning spreading resistance and scanning capacitance measurements to reveal the inhomogeneous doping profiles created by the electric field. © *1998 American Institute of Physics.* [S0003-6951(98)03539-6]

Even though complementary metal–oxide–semiconductor (CMOS) technology dominates modern integrated circuits, bipolar junction transistors (BJTs) remain important components in the electronic industry. Therefore, with increasing circuit miniaturization, the question of limits to downscaling of BJTs arises. Earlier we demonstrated how thermally assisted electromigration (TAEM) of dopants can yield BJT structures 10's of μm in size in Li- and Cu-doped Si and in $CuInSe_2$ (CIS).[1] The relatively mild conditions of TAEM provide an experimental handle to investigate these limits. Because a BJT is a space-charge-limited device, its minimal size will be governed by the dimensions of the space-charge regions, which in turn, can be related to the electric screening properties of the semiconductors.

We can estimate the minimal size of BJT structures as follows. For a device to function as a space-charge-controlled one, the electric field due to the junctions should influence electron transport across them. Thus, the junctions should have a minimal width of several Debye (electric screening) lengths, L,[2] on each side. For a typical semiconductor with a majority carrier concentration of $\sim 5 \times 10^{17}$ cm^{-3} and a relative dielectric constant of 10, $L \sim 5.5$ nm. Considering a minimum of $1L$/depletion region for the outer (emitter/collector) region and of $3L$ for the inner (base) one, the minimum size of the device structure should be $5L$ (28 nm). The geometry of the TAEM experiment leads to hemispherical BJT structures.[1] In cross section these are $p/n/p^+/n/p$ structures, i.e., they consist of four junctions (two each of p^+/n, and of n/p). Thus, their minimum cross section will be $\sim 10L$, for the model system.

To check and demonstrate the lower limits for the space-charged-based devices, we used atomic force microscopy (AFM) with an electrically conducting tip of either doped diamond or oxidized gold (see below), to induce TAEM in the bulk of $CuInSe_2$.[3]

n-CIS single crystals were grown by the traveling heater method (THM), converted to *p* type, and characterized by various methods (see Ref. 4 for details). Experiments were done on surfaces that had been freshly cleaved in air or N_2. We used two methods to obtain electrical contrast in the AFM-based measurements: capacitance and spreading resistance. In scanning capacitance microscopy (SCM),[5] space-charge regions can be imaged. Contrast in scanning spreading resistance (SSR)[6] images results from differences in doping concentration and mobility.

For SCM we used an oxidized gold AFM tip in a commercial SCM instrument.[7] The local AFM-based differential capacitance signal is a qualitative one, proportional to the amount of the free carriers that exist in the sample.[5]

Figure 1(b) shows the SCM image of a BJT structure with a 0.5×0.7 μm elliptical cross section, in a *p*-CIS crystal ($p = 2.5 \times 10^{17}$ cm^{-3}), created by applying a -12 V bias pulse to the sample, followed by SCM scanning. Figure 1(a) is the corresponding topographic image showing a small indentation (<1 nm) forced in the process. In the capacitance signal, the p/n and n/p^+ space-charge regions are observed clearly as dark fringes around the bright ring [p^+/n and n/p regions in the *n* layer; Fig. 1(b)]. Under our experimental conditions (probe size, voltage range, carrier density) we estimate an optimal resolution of ~ 50 nm. As can be seen from the image, this will limit use of SCM for smaller structures of this type.

SSR can in principle provide higher spatial resolution. AFM-based SSR is measured using a sharp conducting tip[8] to define a contact area A that is sufficiently small so that the main contact resistance R is large compared to all the other resistances in the circuit (back contact, bulk crystal, etc.). R can be estimated as:[6,9]

$$R = \frac{\rho}{4} \sqrt{\frac{\pi}{A}}, \tag{1}$$

where ρ is the local resistivity and A is the contact area. This can be justified using a typical value for ρ(1–10 Ω cm), and with A determined using a Herzian model[10] as 10^{-15} m^2, to give R in the range of MΩ, which is indeed orders of magnitude larger than other system resistances. Thus, the SSR measurement is related mainly to the contact resistance. The

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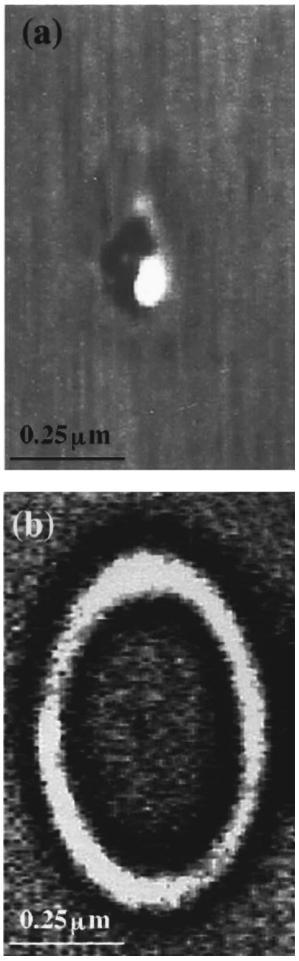

FIG. 1. AFM (a) and scanning capacitance (b) images of a transistor structure in p-$CuInSe_2$ (CIS). To create the structure, a single pulse, -12 V was applied to the sample for 0.1 s. CIS samples were biased using the AFM tip as front and Ag paste as back contacts. (a) Topographic scan, exhibiting minor damage in the center which is not reflected in the capacitance image. The faint dark ellipse which conforms to the central region of (a) would be consistent with an apparent height of <1 atomic step and hence reflects false topography due to force fluctuations arising from the subsurface charge. (b) Differential capacitance (magnitude) image of the same area. The inner p^+ part is surrounded by a bright ring which corresponds to the n region. The outside area corresponds to the bulk p-type sample. The dark stripes surrounding the ring are the space charge regions (no free carriers are imaged).

current measurements are then proportional to the local resistivity of the sample which scales with the local electrical properties. Thus, the SSR image reflects the local conductivity type under the scanning tip.

Biasing a p-CIS crystal by a single pulse (-10 V for 0.1 s) led to the formation of sub-μm sized structures. Figure 2(b) shows the smallest device structure that we observed. The $p/n/p^+/n/p$ structure was formed with no corresponding topographical changes [Fig. 2(a)].

Because SSR characterization is essential in this experiment, we checked its validity by comparing the SSR images to electron beam-induced current (EBIC) ones, as EBIC has a proven ability to detect the internal electric fields in p/n junctions.[1] A comparison of the EBIC with the SSR image of a large structure (10–20 μm in diameter) showed one to one correspondence between the two methods.[11] This justifies using SSR on submicron device structures, which are beyond the EBIC resolution.[12]

To be able to compare the size of the smallest device

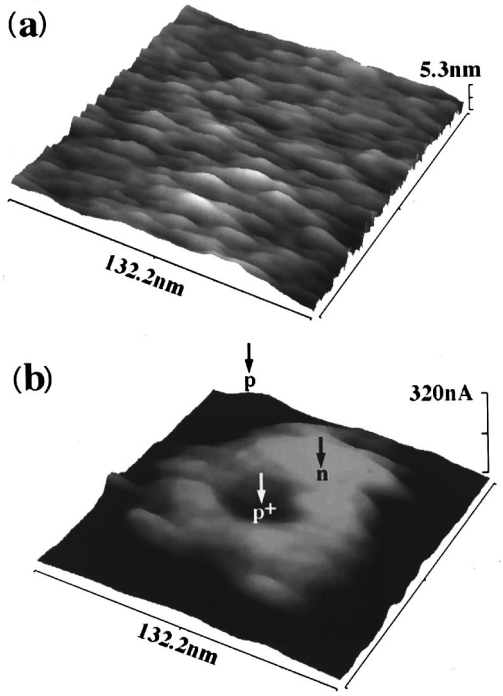

FIG. 2. AFM (a) and scanning spreading resistance (b) images of another sub-μm device structure in p-CIS, created by applying a single -10 V sample pulse for 0.1 s. The p, n, and p^+ regions are labeled in the SSR image.

structure to the minimum size predicted by the earlier given screening length approach, we need to calculate the Debye length. For this we use a static dielectric constant of 13 for CIS[13] and the experimentally determined carrier concentration of the crystal ($p=2.5\times10^{17}$ cm^{-3}). We estimate the p^+ carrier density as 10^{18} cm^{-3}. Using n as a free parameter we find $L=8.7$, 6.2, or 4.4 nm for $n\sim2.5\times10^{17}$, 5×10^{17}, and 10^{18} cm^{-3}, respectively. These values correspond to minimum diameters for the $p/n/p^+/n/p$ structures of $\sim$90, 60, and 45 nm, respectively. From Fig. 2(b) we find the diameter to be 90 nm.

A final issue is the applicability of TAEM to such small systems. It was shown[1] that in the case of CIS, the conditions needed for the process are electric fields on the order of 10^5 V/cm and a $\sim$200 °C increase in the local temperature. To check whether such a mechanism can be operative for the conditions under which the sub-μm device structures were fabricated with AFM, we estimate the electric field distribution and magnitude, and the temperature increase during the experiment.

Assuming a small Schottky barrier contact (spreading resistance) one can show that more than 80% of the applied voltage drops across a region which is about five times the contact radius.[9] Since the contact radius in the AFM experiment was $\sim$20 nm,[8] the main voltage drop will be within a radius of 100 nm. The magnitude of the average electric field can be estimated using Ohm's law in spherical coordinates:

$$E=-\frac{I}{2\pi\sigma R^2}, \tag{2}$$

where I is the current, σ is the local conductivity, and R is a spherical coordinate. Choosing $I=1-2$ μA (average value of current measured during the experiments, such as those

yielding the results of Fig. 2), $\sigma = 5 \times 10^{-4}\ \Omega^{-1}\ \mathrm{cm}^{-1}$ (estimation of the conductivity of the biased barrier), we find from Eq. (2) an average electric field of 10^6 V/cm, which exceeds that needed to induce the process.

The temperature increase during the voltage pulse must be high enough to allow ion diffusion, but low enough to avoid surface melting. One can estimate the increase of the local temperature under the tip as[9]

$$\Delta T = \frac{0.5P}{\pi k_{\mathrm{th}} R_0}. \tag{3}$$

Here, P is the average power dissipated around the contact, k_{th} is the thermal conductivity, and R_0 is the spherical contact radius, which is orders of magnitude smaller in the AFM experiment than in the previous experiments,[1] where we had little control over the contact area. Using typical values of power measured during the process (0.15–1 mW), and $k_{\mathrm{th}} = 0.1$ W/(cm °C) (see Ref. 1) and $R_0 = 20$ nm, we find from Eq. (3) $\Delta T \sim 120-800$ °C. Indeed, in some extreme cases of high power injection, local surface melting was observed (the bulk melting point of CIS is 1100 °C). Therefore we conclude that under these experimental conditions sub-μm sized junctions can be created by the same mechanism as is thought to be responsible for larger scale device creation, viz. thermally assisted electromigration of dopants.

Assuming the mobile dopant to be a Cu-related defect[14] and n to be $2.5 \times 10^{17} - 2.5 \times 10^{18}\ \mathrm{cm}^{-3}$, we can calculate that the maximum number of defects that can be involved in the process leading to the structure shown in Fig. 2(b), will be less than 150! We note that this number is insufficient to generate the $\alpha \rightarrow \beta$ phase transition in $CuInSe_2$.[15]

In summary, we have demonstrated that TAEM can create sub-μm transistor structures using AFM. With this method we showed the ability to create and image device structures close to the lower limits of their physical sizes.

D. Cahen thanks the Israel Science Foundation, Minerva foundation, Munich, German-Israel Foundation for Science and Development (GIF) and the Israel-EU research program through the Israel Ministry of Science for partial support. The authors thank A. Erickson (Digital Instruments, Santa Barbara, CA) for working with S. Richter to obtain the scanning capacitance images. Yishay Manassen holds the Lilian and George Lyttle Career Development Chair.

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